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Title- **A Continuous Service Real Time Clock for Digital Computers**

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ABSTRACT

A low cost, "continuous service" time base generator has been designed to provide a reliable date/time function for digital computers. The term "continuous service" as applied here means that the clock continues to keep time during power blackouts, system failures and shutdowns, and can be read whenever the computer is operable. The circuit description includes a simple interface to the PDP-11 family of computers.

Pages Text 3	Other 5	Total 8	
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Subject: **A Continuous Service Real Time Clock for Digital Computers**

Case- 39199 -- File- 39199-11

date: **March 13, 1975**

from: **J. R. Vollaro**

TM: **75-1273-4**

MEMORANDUM FOR FILE

INTRODUCTION

A "continuous service" time base generator has been designed to provide a reliable date/time function for digital computers. The term "continuous service" as applied here means that the clock continues to function during power blackouts, system failures and shutdowns and can be read whenever the computer is operable.

Time is recorded by a 36 bit binary counter which is incremented at 1 second intervals by a timer. The second count is synchronized to local time and converted to the desired units (years, months, days, etc.) by appropriate software.

To provide continuous service the timer must keep running and the count remain unaltered during computer hardware, software, and power failures. Powering the timer and counter circuits from an independent source isolates the clock from the effects of AC power failures. A rechargeable (nicad) battery is used for this purpose and is charged from the AC power line when it is available. The counter and timer have been implemented with Cos-Mos integrated circuits to reduce the power required to sustain operation during AC power failures. Constant battery recharging and the low power requirements of the circuitry allow specification of a small battery which is mounted on the circuit board to reduce the chance of accidental disconnection. A penlight sized 5V battery powers the counter and timer for 36 hours without recharging.

The one second timer must be very precise or error compensated to prevent a large error build up over long periods of time. Since it is not practical to battery power the oven and regulated power supply necessary to support a high precision crystal oscillator, an efficient (less accurate) crystal oscillator is used as the frequency source only when the power line is not available. When AC power is available, (more than 99% of the time) the error compensated line frequency is used to control the timer. Switching between frequency sources is automatic and does not affect the period of the timer.

The clock has been implemented as a read only device to avoid inadvertent alteration of the count through computer hardware or software failures. External hardware or a software offset must be used to synchronize the count with local time.

The timer provides a buffered 60 hz output which is used to drive a 6 digit time display. The display is a commercially available digital clock which was modified to accept its 60 hz timing signal from an external source. When connected to the timer, it provides a synchronous display of the time of day as recorded in the time base.

Interfacing

The clock has been interfaced to a PDP-11 computer through a DR11C general purpose interface module. The DR11C has TTL input characteristics and a 16 bit format. These requirements and the interface timing functions are accomplished on the clock circuit board with TTL logic that is powered by the computer.

A 2:1 multiplexer is used to map the least significant 32 bits of the count into two 16 bit halves. The upper and lower halves are selected for reading under program control and read into 2 PDP-11 words.

Reading the count in two parts presents the following problem. If the count is updated between readings, and the update results in a carry between the lower and upper halves, (major transition), the total reading reflects a 16 bit error. Logic has been included in the interface which guarantees a correct reading if both halves are read within one second. If the two halves are not read within 1 second, the possible error must be dealt with in the software.

A flip flop which is set by the 60 Hz clock is connected to the interrupt line of the DR11C to provide a 60 Hz interrupt. The flip flop is reset by one of the read instruction function bits.

The two bit function field of the DR11C is coded as follows:

00 Read the least significant half of the counter.

01 Read the most significant half of the counter.

10 Read the least significant half and reset the 60 hz. interrupt flag.

11 Read the most significant half and reset the 60 hz. interrupt flag.

Physical Description

The clock circuits and TTL interface logic reside on the 7" x 10" printed circuit board shown in Figure 1. The battery, crystal and other discrete components are mounted in a 2" margin at the left side of the board. An aluminum cover helps to protect the component side of the board from physical damage.

The I/O connections are located at three 16 pin DIP connectors on the right edge of the board (IC-6, 18, and 30). The pin connections are listed below.

NAME	CLOCK	DR11C
INIT	30-11	1-P
DTR	30-10	2-C
CSR0	30-13	2-K
CSR1	30-9	1-DD
REQA	18-10	2-S
IN-00	6-15	2-TT
IN-01	6-13	2-LL
IN-02	30-12	2-H
IN-03	18-16	2-BB
IN-04	6-12	2-KK
IN-05	6-11	2-HH
IN-06	6-10	2-EE
IN-07	6-9	2-CC
IN-08	18-15	2-Z
IN-09	18-14	2-Y
IN-10	18-13	2-W
IN-11	18-12	2-V
IN-12	18-11	2-U
IN-13	30-16	2-P
IN-14	30-15	2-N
IN-15	30-14	2-M

Circuit Description

Refer to the schematic diagram (Figures 2 and 3) for the following description.

The primary of T1 is connected to the 110V AC line voltage. Its outputs are used to sense the presence of AC power, (ACON+), develop the 60 Hz line clock, (LINCO-), and to charge the nicad battery. The battery is the source of V1 (V1 = +5 volts) which powers the Cos Mos logic modules. Charging current for the battery is provided by T1 through CR1 and R11.

Y1 and an inverter section of IC 12 produce a 60 KHz output which is reduced to 60 Hz by 3 decade counters in tandem (IC 36, 48, and 60). IC 35 selects the AC line frequency (LINCO+) as the 60 Hz source when the AC power is on (ACON+), or the crystal controlled source (XTLCO) when the power is off. IC 23 divides the 60 Hz source by 60 to produce the 1 second function (1 Hz-) and (1 sec +). The 1 second transitions are counted by IC 47, 59 and 71 which are 12 bit counters (figure 3).

The contents of the counter are transferred to a TTL register (IC 9, 21, 33, 45, 57, and 69) at 1 second intervals after the counters have settled. Register load pulses (LOAD+) are inhibited while a read is in progress to avoid transient errors. Register updating is also inhibited for 1 second (MHOLD-) if a read is issued during a major transition. A compatible pair of readings is guaranteed if the second half is read during the period of MHOLD.

Conclusion

The establishment of a reliable, accurate and continuous time base usually requires elaborate hardware. The relatively simple circuits described here provide a similar service by supplementing the accurately controlled and almost continuous AC power source with a battery powered source.

The prototype has been in operation for about a year on a computer which serves as a file store in a network of computers. Its time function is provided as a service to the other computers in the network via the file store. Four of these computers access the clock automatically upon rebooting and use the time function to resynchronize their internal clocks with the correct date and time.

J. R. Vollaro

MH-1273-JRV-UNIX

Att.
Figures 1-3
Photo No. B75-1580-MH

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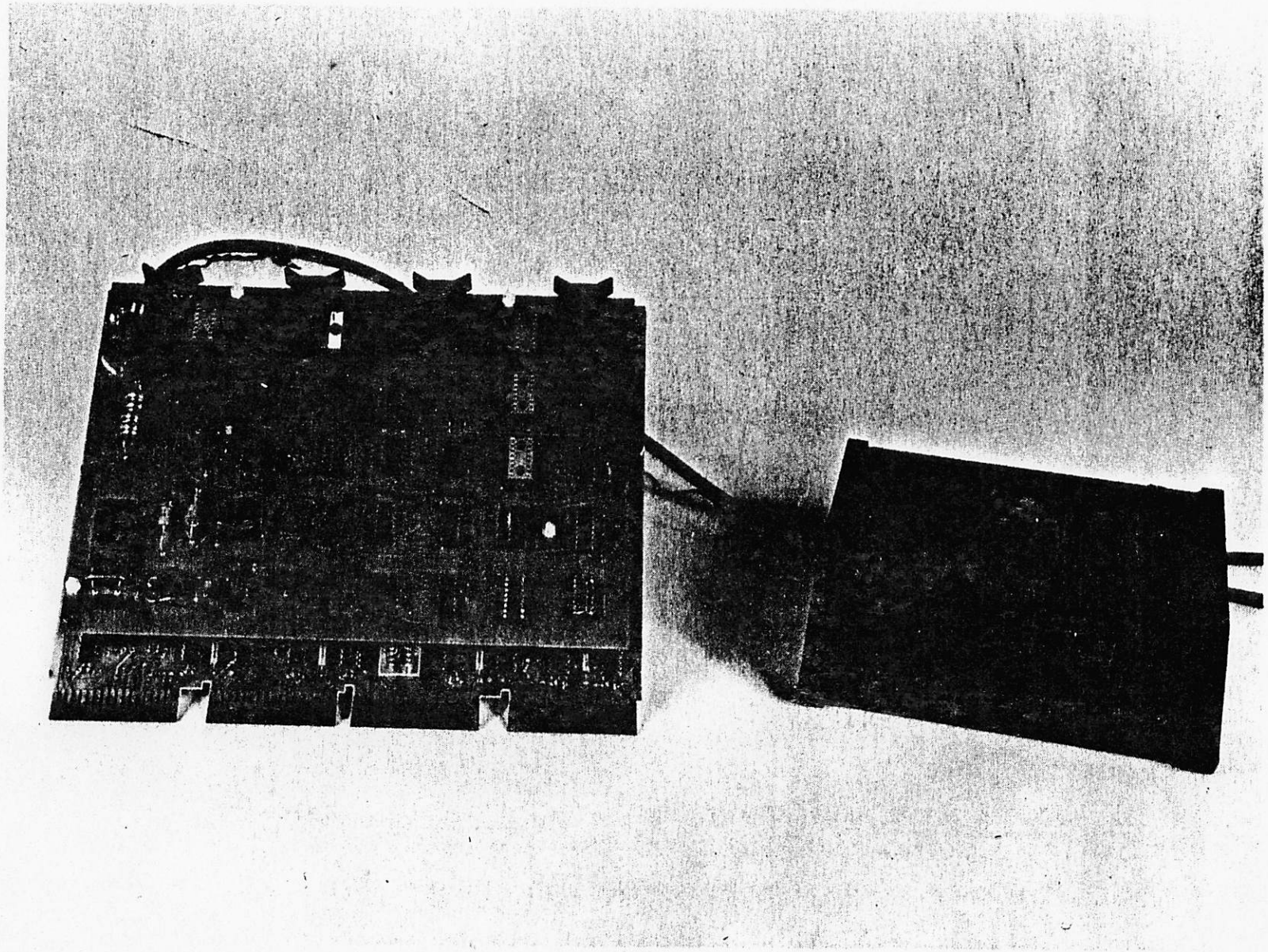

Figure 1

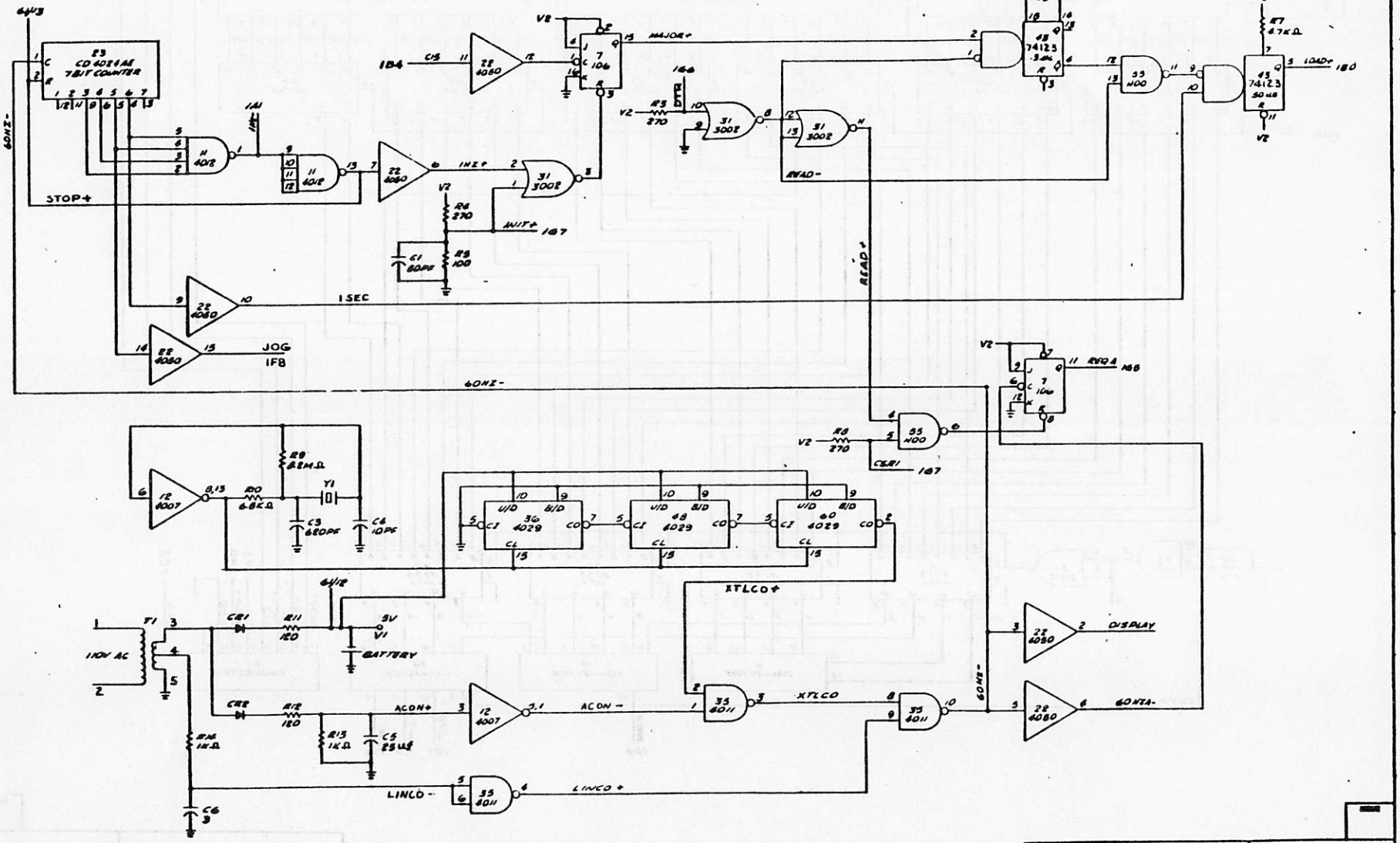

FIGURE 2

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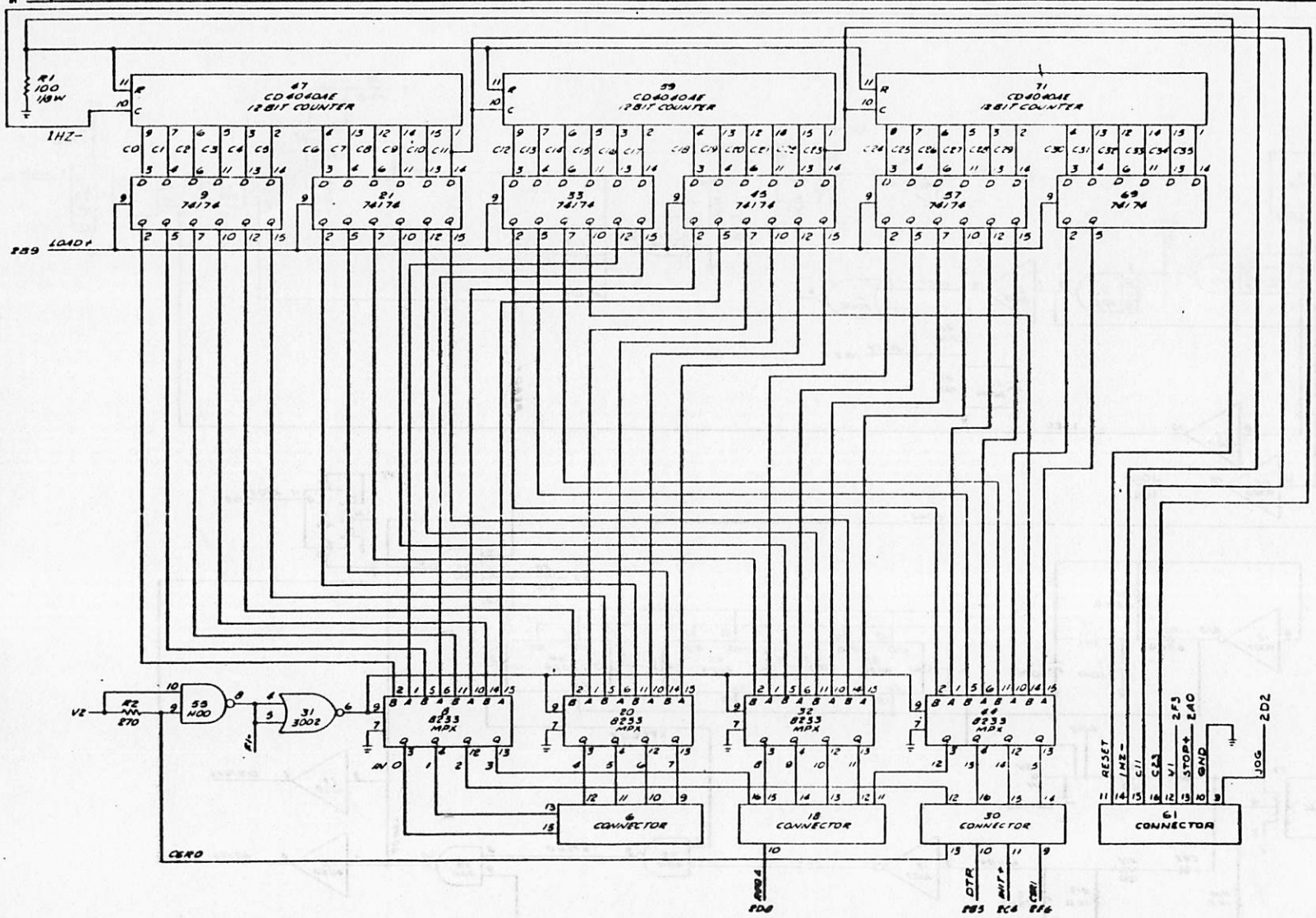
R1
100
1/8W
1HZ-
47
CD4040AE
12 BIT COUNTER
59
CD4040AE
12 BIT COUNTER
71
CD4040AE
12 BIT COUNTER
9
74174
21
74174
33
74174
45
74174
57
74174
69
74174
LOAD+
R2
270
5
NOT
31
3002
8
8233
MPX
20
8233
MPX
32
8233
MPX
44
8233
MPX
6
CONNECTOR
18
CONNECTOR
30
CONNECTOR
61
CONNECTOR
RESET
1HZ-
STOP+
GND
2D2
ZERO
DTR

FIGURE 3